Docket No. 214400US-2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Yasuo YAMAGUCHI

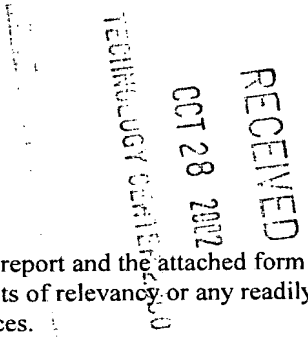
SERIAL NO: 09/964,462 GAU: 2827

FILED: September 28, 2001 EXAMINER: L. Cruz

FOR: SEMICONDUCTOR DEVICE

INFORMATION DISCLOSURE/RELATED CASE STATEMENT UNDER 37 CFR 1.97

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231



SIR:

Applicant(s) wish to disclose the following information.

REFERENCES

- ☐ The applicant(s) wish to make of record the references listed on the international search report and the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

- ■ Attached is a list of applicant's pending application which may be related to the present application. A copy of the claims and drawings of the pending application is attached.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

- ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ■ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

- ■ Please charge any additional fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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Robert T. Pous
Registration No. 29,099

LIST OF RELATED CASES

Docket Number	Serial or Patent No.	Filing or Issue Date	Status or Patentee
214400US2*	09/964,462	09/28/01	PENDING
225729US2	10/208,993	08/01/02	PENDING

*Present application; listed for information

GJM/ae

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WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate having a major surface;

an isolation insulating film selectively formed on said major surface;

a resistor layer formed on said isolation insulating film;

an interlayer insulation film covering said semiconductor substrate, said isolation insulating film and said resistor layer;

first and second interconnection layers disposed on said interlayer insulation film;

a first conductive plug selectively buried in said interlayer insulation film and having an upper end connected to said first interconnection layer and a lower end connected to one end of said resistor layer and a first portion of said major surface of said semiconductor substrate which is adjacent to said isolation insulating film,

said first conductive plug being rectangular in cross section along said major surface with its long sides extending along a main direction to connect said one end and the other end of said resistor layer and its short sides extending along a direction orthogonal to said main direction; and

a second conductive plug selectively buried in said interlayer insulation film and having an upper end connected to said second interconnection layer and a lower end connected to said other end of said resistor layer.

2. The semiconductor device according to claim 1, wherein

said lower end of said second conductive plug is also connected to a second portion of said major surface of said semiconductor substrate which is adjacent to said isolation insulating film, said second portion being opposite to said first portion through

said isolation insulting film, and

said second conductive plug is rectangular in cross section along said major surface with its long sides extending along said main direction of said resistor layer and its short sides extending along said direction orthogonal to said main direction.

3. The semiconductor device according to claim 1, wherein

a distance along said major surface and between one end of a connection of said first conductive plug and said major surface which is in contact with said isolation insulating film, and said one end of said resistor layer is set to equal to or less than approximately a value of a design rule for said semiconductor device.

4. The semiconductor device according to claim 1, wherein

a distance along said major surface and between one end of a connection of said first conductive plug and said major surface which is in contact with said isolation insulating film, and said one end of said resistor layer is set to equal to or less than approximately twice a thickness of said resistor layer.

5. The semiconductor device according to claim 1, wherein

said semiconductor substrate comprises a first semiconductor layer of a first conductivity type and a second semiconductor layer of a second conductivity type selectively formed on said major surface, said first and second semiconductor layers forming a pn junction therebetween, and

said lower end of said first conductive plug is connected to said second semiconductor layer.

6. The semiconductor device according to claim 5, wherein

a width of said second semiconductor layer along said main direction of said resistor layer is set to approximately a value of a design rule for said semiconductor device.

7. The semiconductor device according to claim 1, wherein

said first conductive plug is divided into a plurality of unit plugs arranged in said direction orthogonal to said main direction of said resistor layer,

said plurality of unit plugs each are rectangular in cross section along said major surface with their long sides extending along said main direction of said resistor layer and their short sides extending along said direction orthogonal to said main direction, a length of said short sides being set to approximately a value of a design rule for said semiconductor device.

8. The semiconductor device according to claim 7, further comprising:

a third conductive plug selectively buried in said interlayer insulation film to couple said plurality of unit plugs which are arranged in said direction orthogonal to said main direction of said resistor layer, and having an upper end connected to said first interconnection layer and a lower end connected to said first portion of said major surface of said semiconductor substrate which is adjacent to said isolation insulating film,

a width of said third conductive plug along said main direction being set to approximately a value of said design rule.

9. The semiconductor device according to claim 7, further comprising:

a fourth conductive plug selectively buried in said interlayer insulation film to

couple said plurality of unit plugs which are arranged in said direction orthogonal to said main direction of said resistor layer, and having an upper end connected to said first interconnection layer and a lower end connected to said one end of said resistor layer,

a width of said fourth conductive layer along said main direction being set to approximately a value of said design rule.

10. The semiconductor device according to claim 1, wherein

a distance of a connection of said first conductive plug and said resistor layer along said main direction is set to more than approximately a value of a design rule for said semiconductor device.

ABSTRACT OF THE DISCLOSURE

A resistor layer (5) is formed on an isolation insulating film (4) selectively formed in a major surface (1S) of a semiconductor substrate (1). An interlayer insulation film (7) covering the resistor layer (5) has first and second plugs (9, 19) buried therein in the form of buried interconnections. The first and second plugs (9, 19) provide connection not only between an end portion of the resistor layer (5) and first and second interconnection layers (8, 18) but also between the end portion of the resistor layer (5) and the major surface (1S) of the semiconductor substrate (1).

FIG. 1

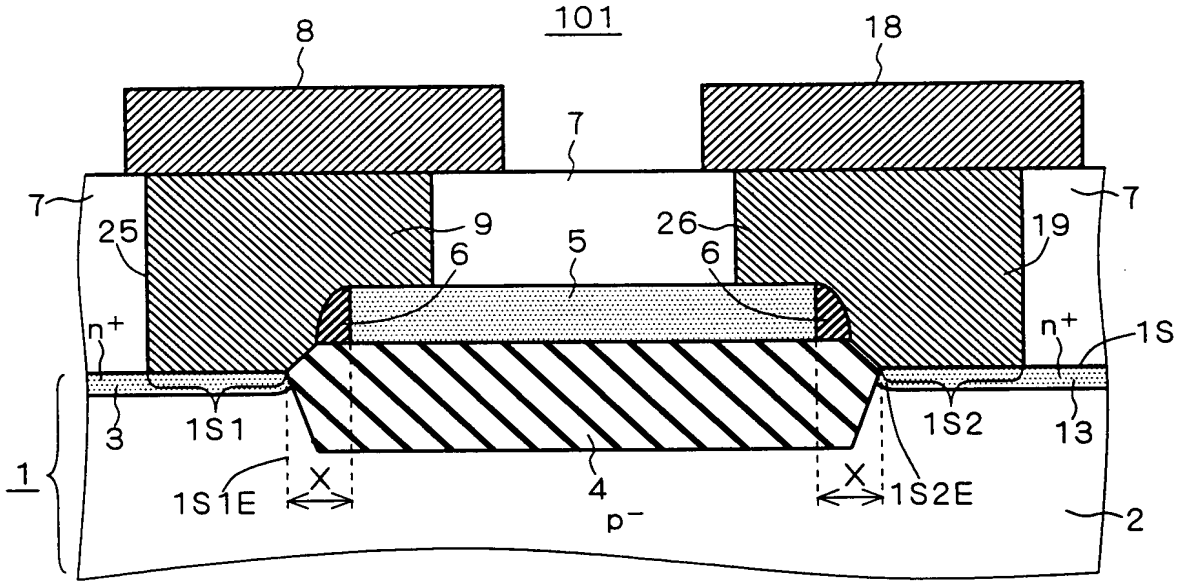

FIG. 2

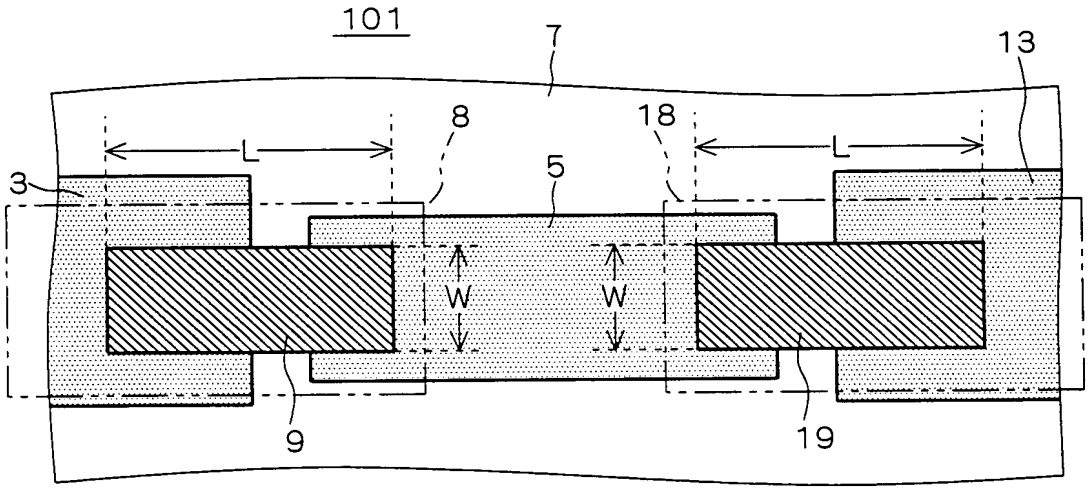

FIG. 3

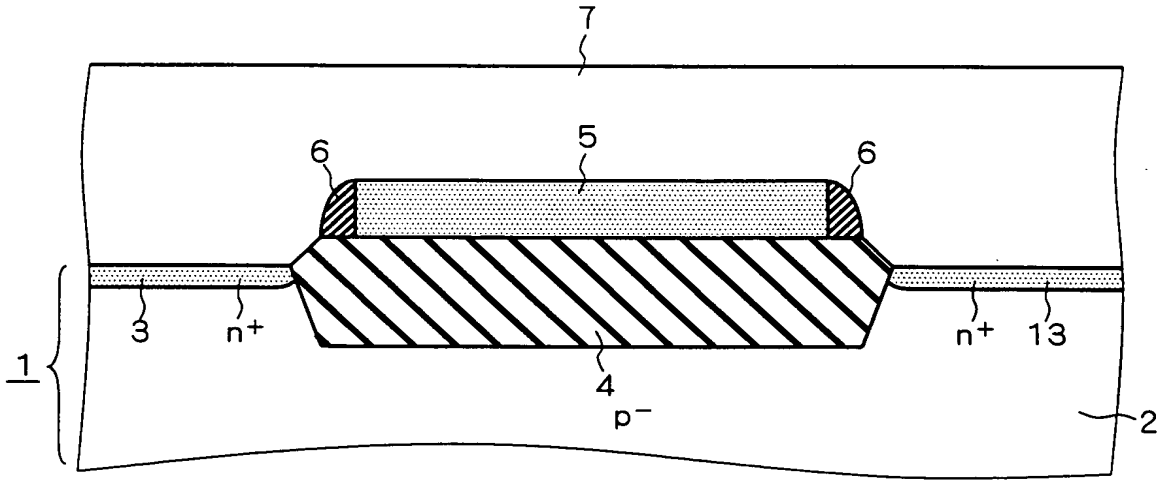

FIG. 4

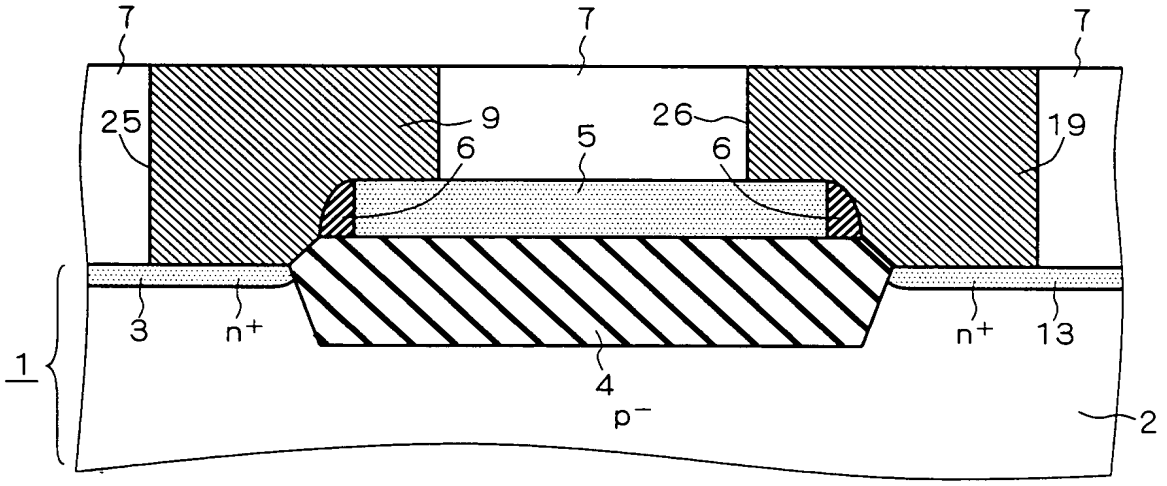

FIG. 5

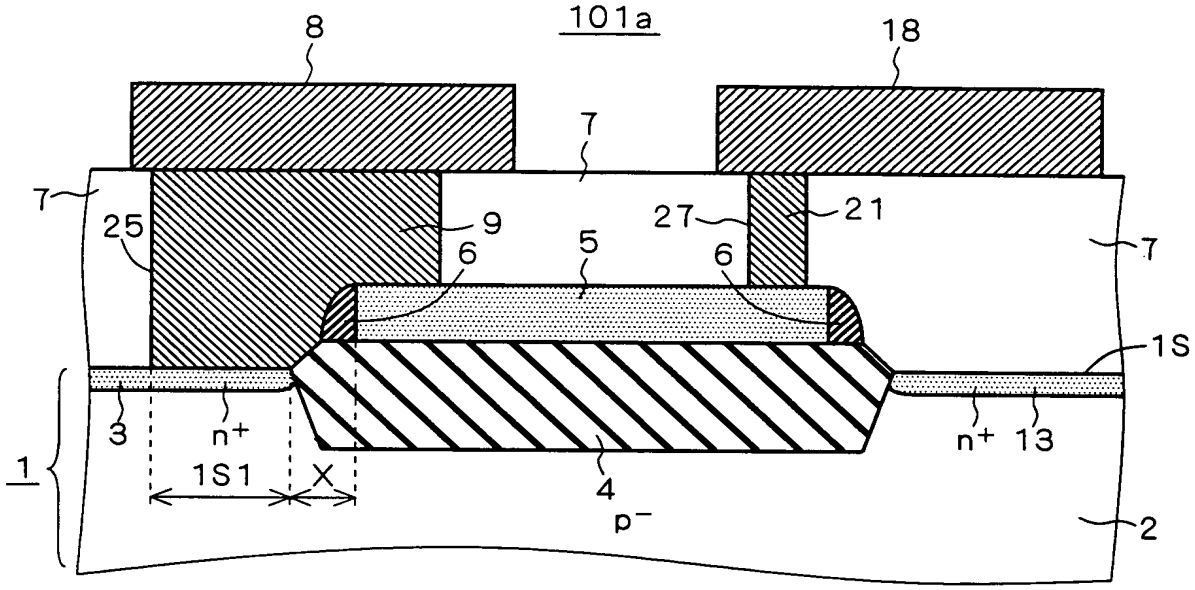

FIG. 6

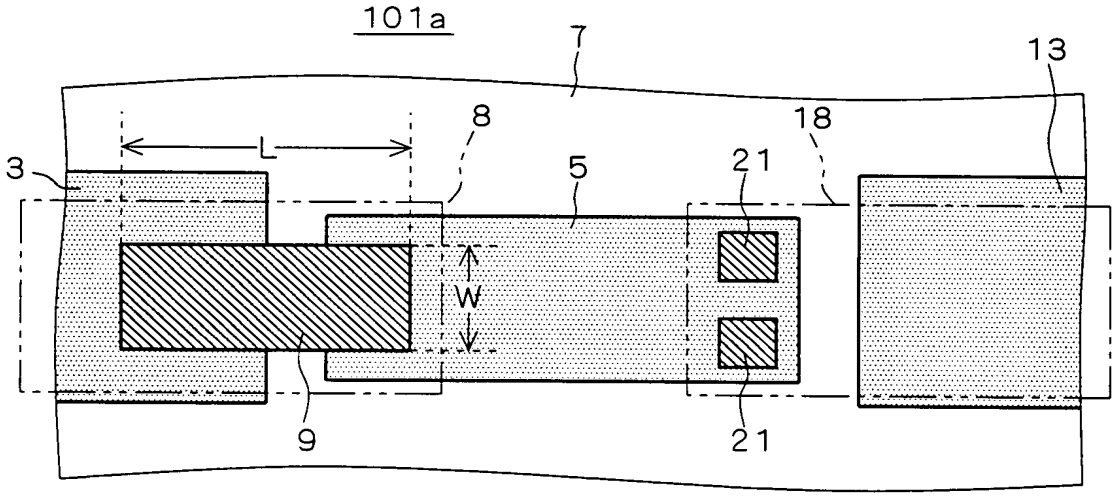

FIG. 7

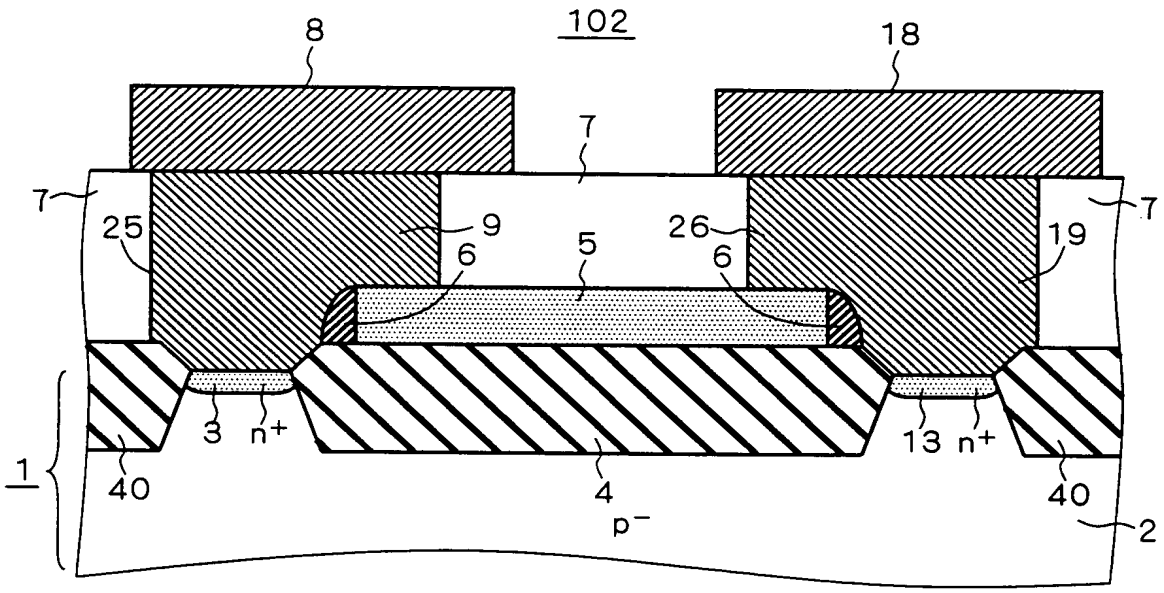

FIG. 8

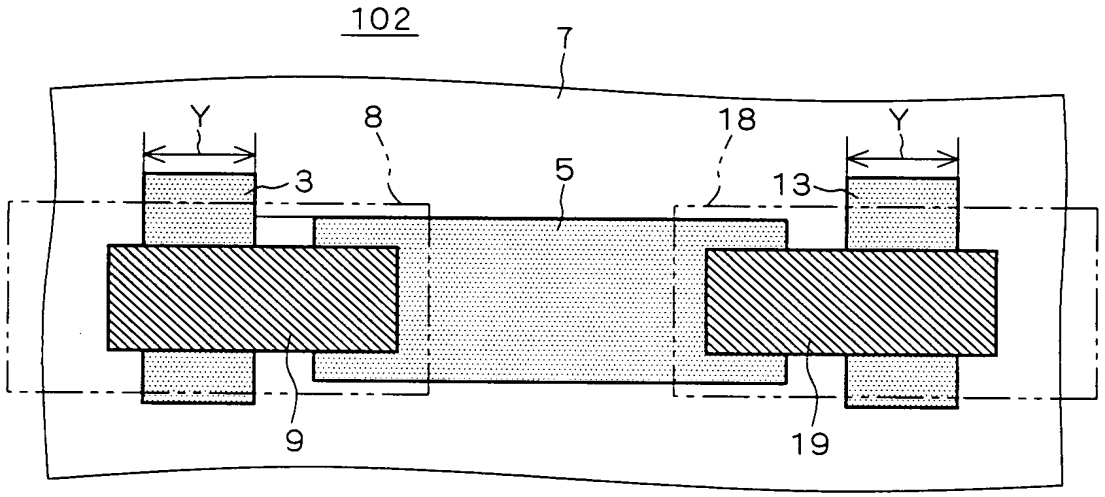

FIG. 9

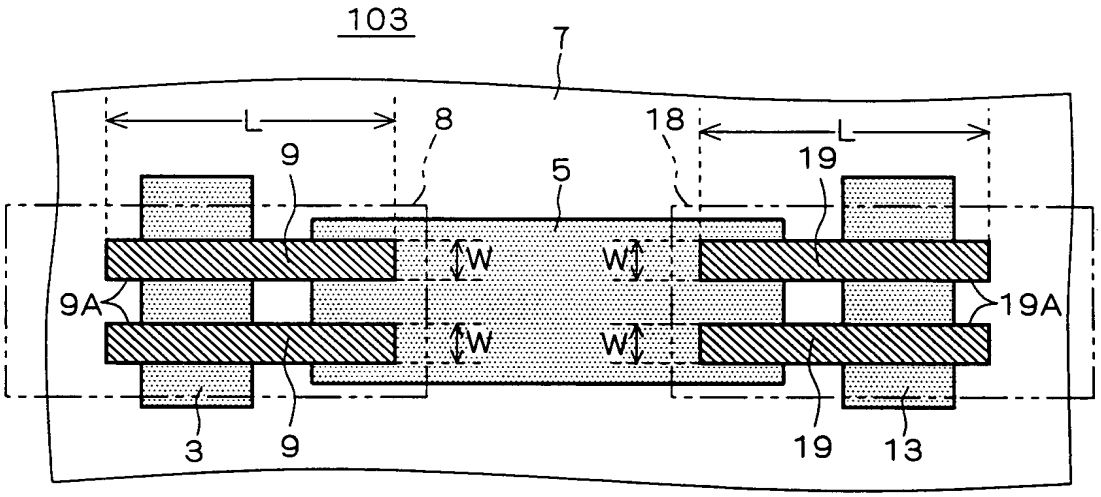

FIG. 10

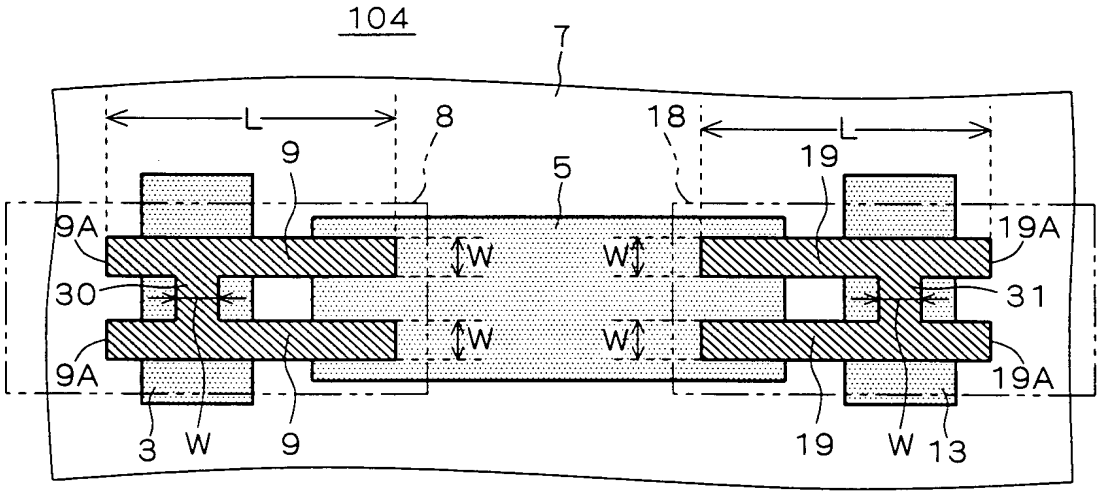

FIG. 11

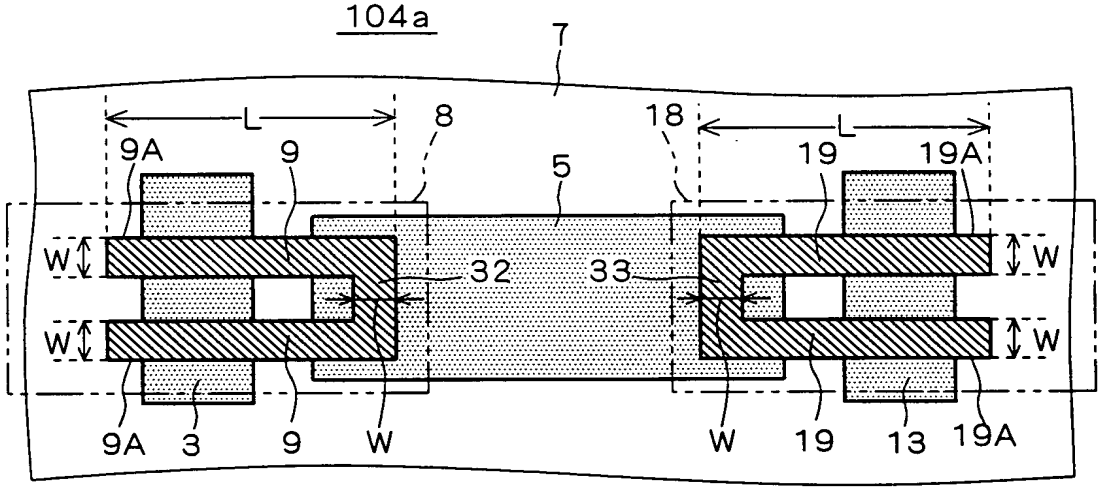

FIG. 12

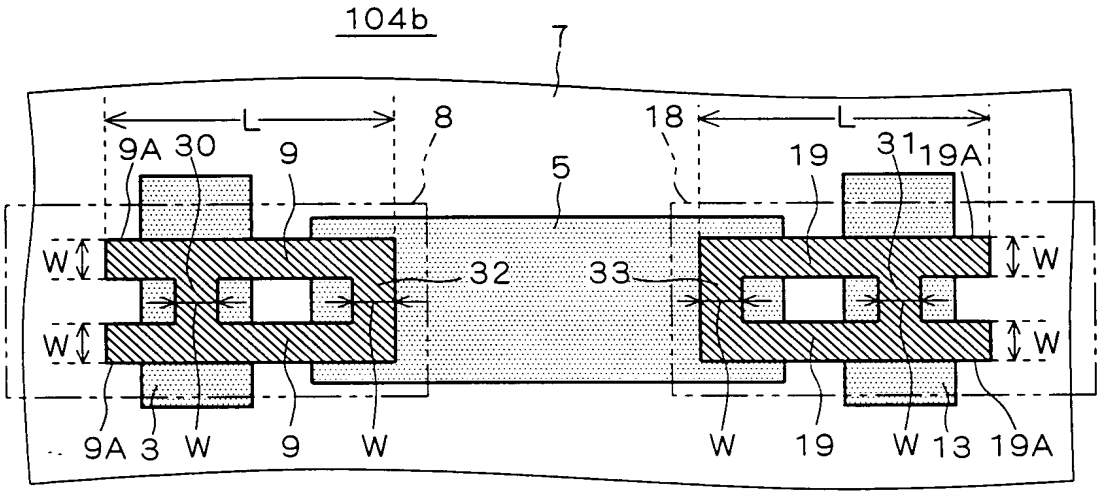

FIG. 13

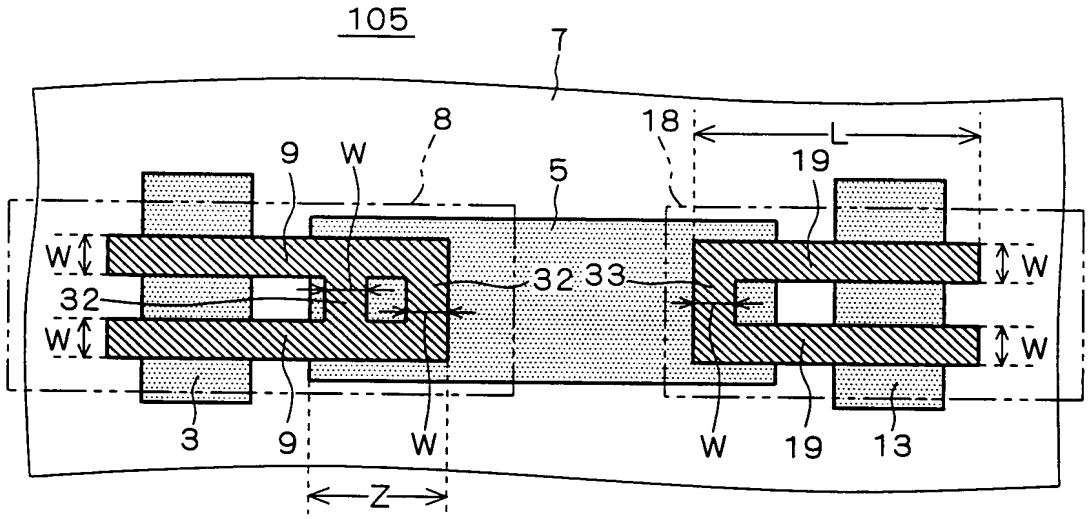

FIG. 14

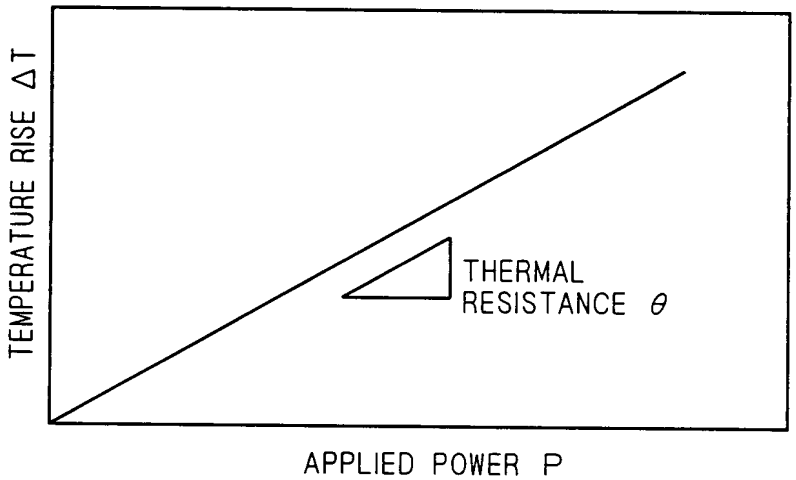

FIG. 15 (PRIOR ART)

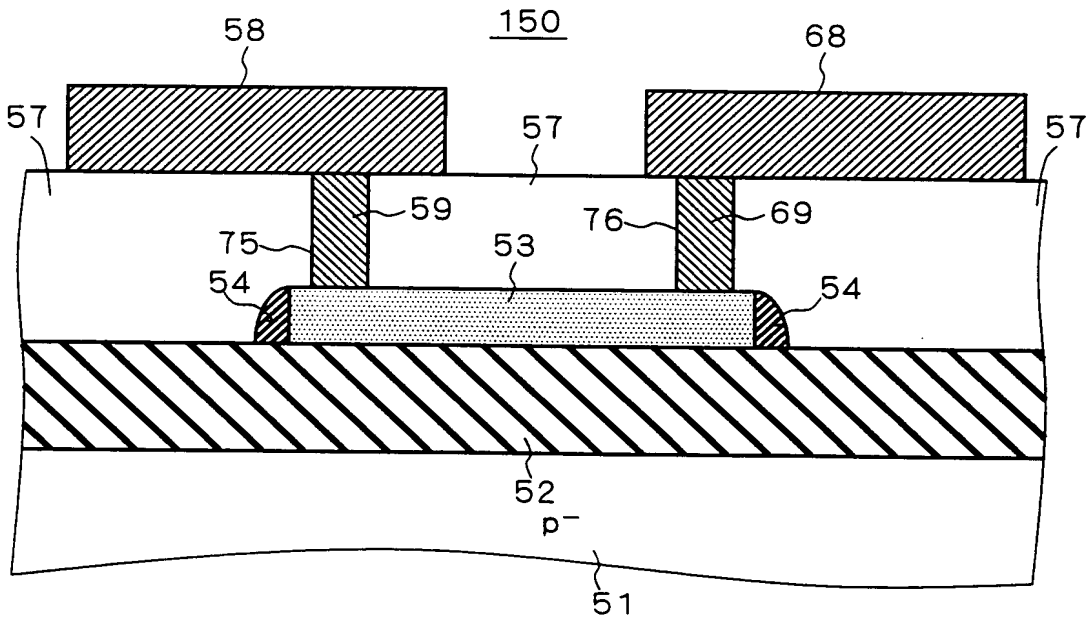

FIG. 16 (PRIOR ART)